IBM Systems and Technology Group

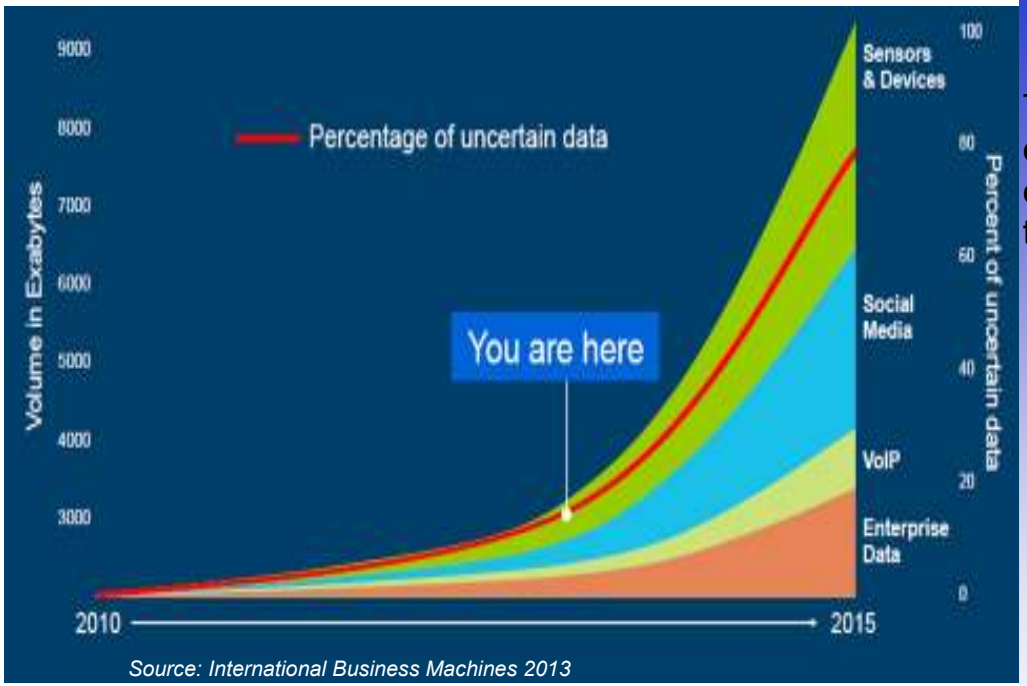
System Scaling Opportunities for Future IT Systems

Jon A. Casey

IBM Fellow
IBM Systems and Technology Group

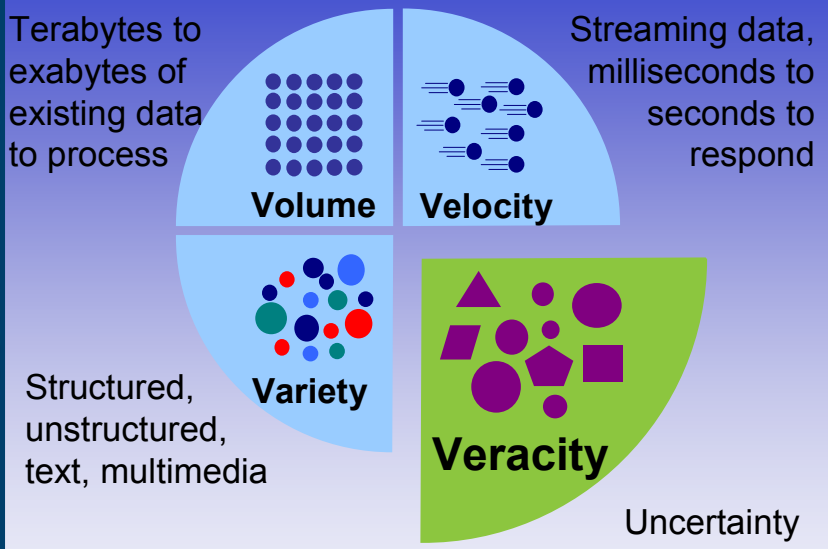
5/24/2014

Data growth will drive the new IT model



Source: International Business Machines 2013

Dimensions of data growth

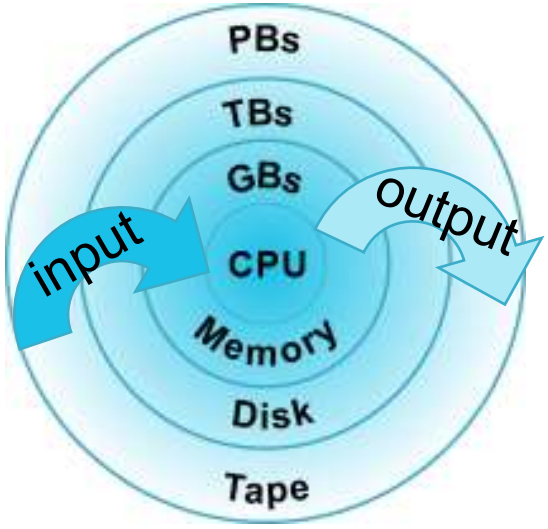


The Data is in the Cloud !

The Compute will move to the Data!

Changes in the compute model –memory centric computing

Old Compute-centric Model

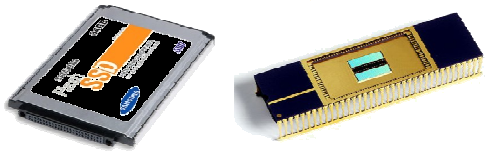


von Neumann architecture

Data lives on disk and tape
Move data to CPU as needed
Deep Storage Hierarchy

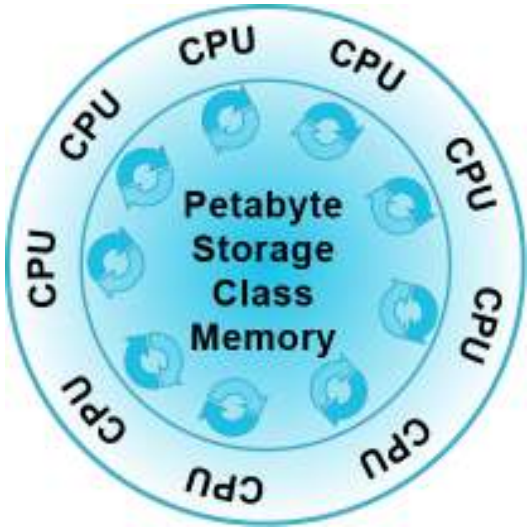
Manycore **FPGA**

Massive Parallelism
Persistent Memory



Flash **Phase Change**

New Data-centric Model



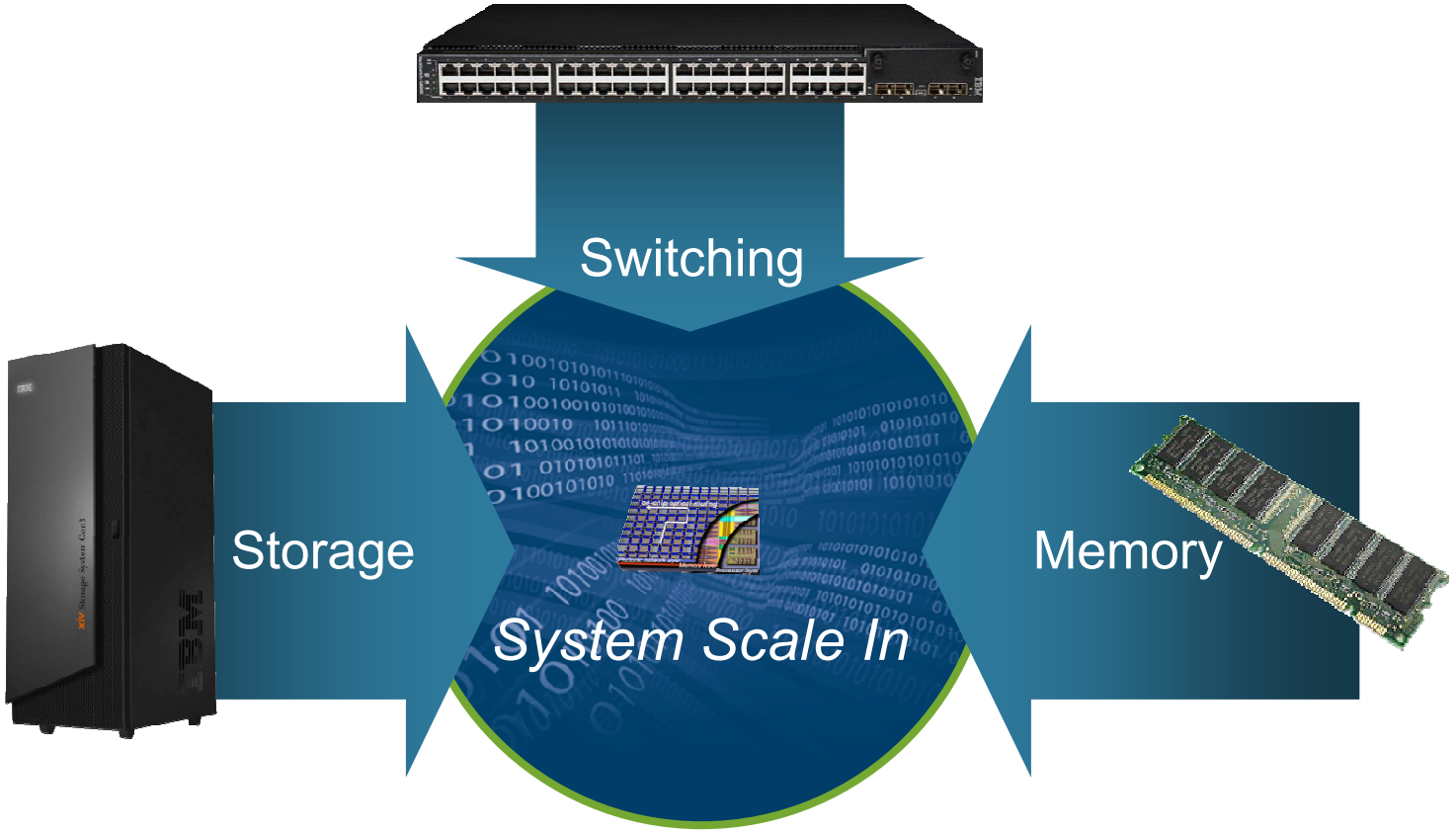
Non von Neumann architecture

Data lives in persistent memory
Many CPU/GPU's surround and use
Shallow/Flat Storage Hierarchy

Huge impact on hardware, systems software, and application design

Open Architecture, Software Defined Environment

A new paradigm for cognitive systems for new workloads

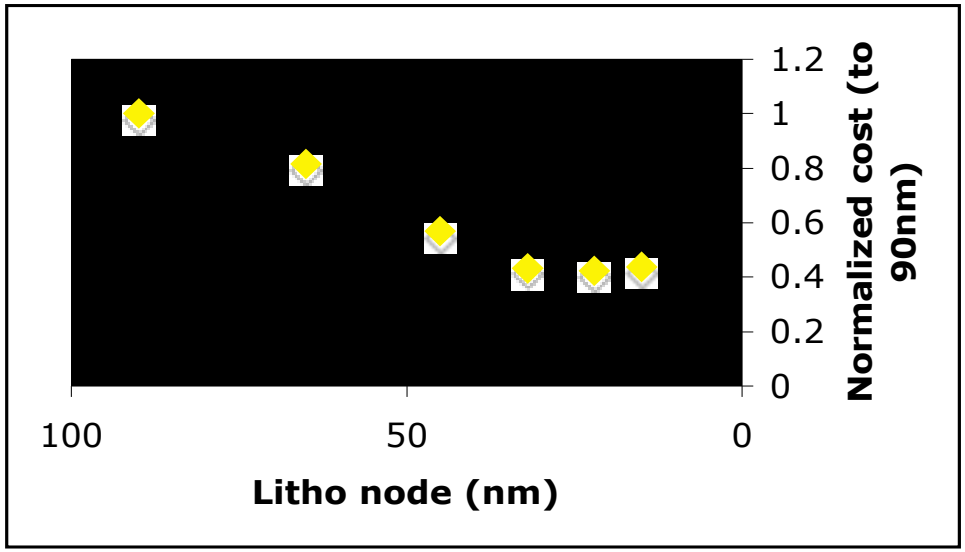


Scale-In Through Silicon and Packaging Innovation

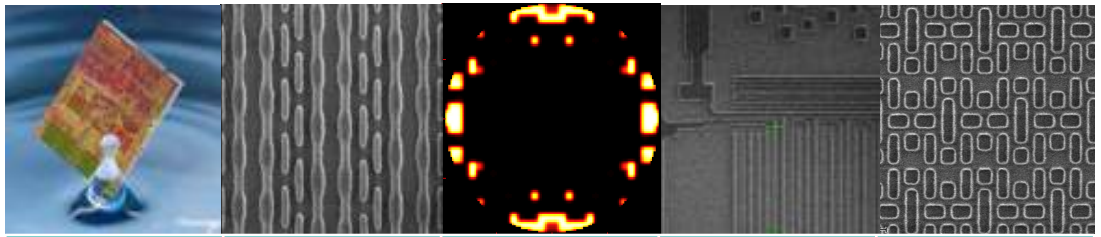
Will Silicon scaling and integration get us to the goal line?

Scaling can and will continue to at least the "7 nm" node

Cost per transistor has begun to saturate



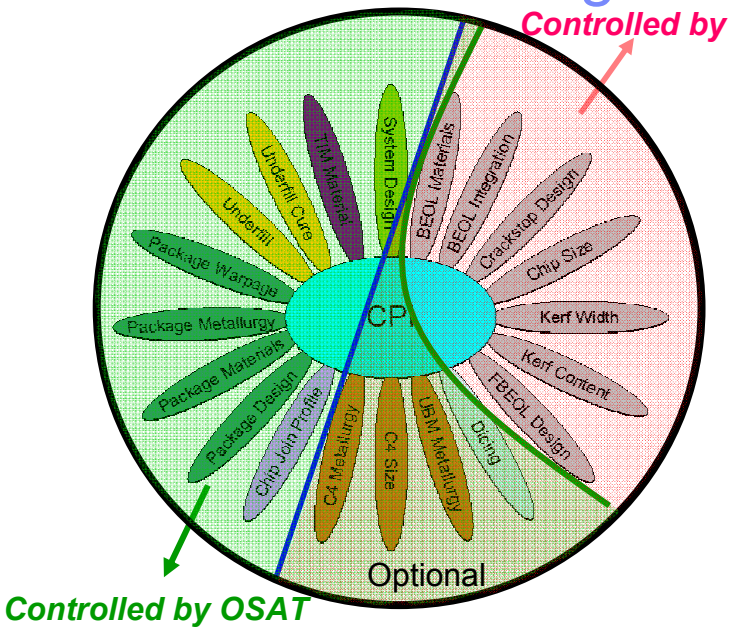
Economics will likely be the key challenge to continued Silicon scaling

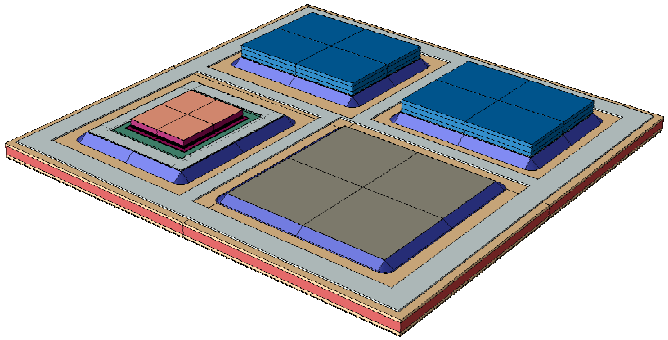


45 nm	32 nm	22 nm	14 nm	10 nm
Immersion (ArFi)	2nd Generation Immersion	3rd Gen ArFi w/ Source Mask Optimization (SMO)	4th Gen ArFi w/ SMO & Double Patterning (DPL)	5th Gen ArFi w/ Multilayer Patterning or EUV

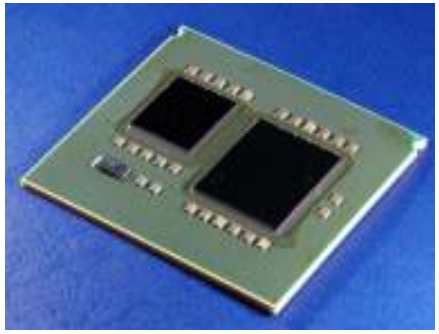
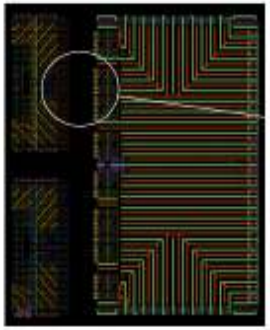
Heterogeneous Integration and 3D*i* : "Volumetric Scaling"

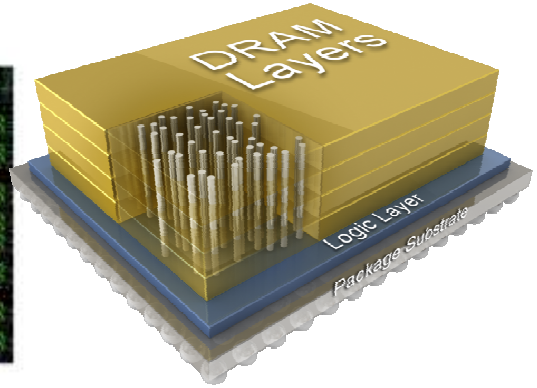
- **Requires co-development of Silicon and Packaging solutions**
  - Packaging is the key technology for volumetric scaling
    - 2D and 3D technologies
    - High performance I/O
    - Optics
    - CPI: Chip-Package Interaction
    - Power and thermal management
- **Provides lower cost solutions to enable system performance**
  - Si cost:performance metric is very challenged
- **Allows for use of mixed semiconductor technologies**
  - Enables use of lower cost technologies for less performance sensitive functions
- **Key Technologies**
  - CSP (chip scale packages)
  - SIP (system in package)
  - Interposers
    - Si and other interposer materials
  - 3D*i*
  - Photonics





MCM, Interposer and 3D Technology for Heterogeneous Integration



	Ceramic MCM	Organic MCM	Si Interposer	Glass Interposer	Organic Interposer	3D
Dielectric Properties	Adequate	Good	Lossy	Excellent	V. Good	Lossy
Feature Dimensions	Mechanically defined	Down to ~10µm L/S	Si-Like Lithography	Display Like	Down to ~5µm L/S	Si Lithography
CTE Induced Stress	V. Good	Mod. High	Excellent	Tailorable	Mod. High	Excellent
Cost	High	Moderate	Moderate	TBD	Low-Moderate	Application Dependent
Availability	Available	Available	Available	Development	Development	Available

L/S = Lines and Spaces

Summary

- **Silicon performance advancement becoming more challenging as scaling is becoming more costly**
  - Need to look beyond CMOS for cost effective technology solutions
- **Integrated co-development of Silicon and packaging solutions required to achieve new technologies with superior cost:performance metrics**
- **Volumetric scaling will be critical to future performance enablement**
  - Tightly coupled modules and components
  - CSP
  - 3D*i* technology
  - Interposer integration
  - High performance I/O and optics

Thank You

Acknowledgements

I would like to thank my colleagues in IBM Packaging, Silicon, Systems and Research for their many contributions

